QUIC_8051
Evaluation Version

Document release 0.9

1 Introduction

This document describes the features and functionality of the evaluation version of the QUIC_8051 embedded controller core. For more detailed information of the QUIC_8051 itself, refer to the appropriate Datasheet, Users Manual and Application Notes.

2 Disclaimer

The evaluation version of the QUIC_8051 is issued "as is". Neither any warranty nor any support is given by Quickchip.

3 License

The evaluation version of the QUIC_8051 core is intended for evaluation purposes only. It is not permitted to build any kind of product based on the evaluation version. It is also not permitted to pass on the evaluation version to anybody without a mention of Quickchip.

4 Compatibility

The evaluation version of the QUIC_8051 core features exactly the same ports as the full version. So, a prototype FPGA design can be made using the evaluation version. Later, only the change of one single file, the net list, is necessary to get a fully functional FPGA. Be aware of the fact that the evaluation version has a smaller footprint and therefore consumes less logic cells than the full version.

5 Peripherals and interrupts

The evaluation version implements the full set of peripherals, e.g. Timers and UART. The peripherals even request interrupts by setting the appropriate request bit. However, the interrupts are not acknowledged by the execution unit. The interrupt request bits (i.e. TF0, TF1, RI etc) can only be polled by the CPU.

6 Supported instructions

The only function the evaluation version is restricted in is the execution unit of the CPU. Some instructions are implemented, some partially, others not at all. Only the instructions listed in table 1 are implemented completely and can be used for programs. Even if some instructions not listed in this table seem to operate properly the might not work under all circumstances.

Table 1. Instructions supported by evaluation version of QUIC_8051

Arithmetic	Data Transfer	Logical	Boolean	Branching
ADD A, Rn	MOV A, Rn	ANL A, #data	CLR C	ACALL
ADD A, direct	MOV A, direct	ORL A, #data	CLR bit	LCALL
ADDC A, Rn	MOV A, #data	CLR A	SETB C	RET
ADDC A, direct	MOV Rn, A		SETB bit	AJMP
SUBB A, Rn	MOV Rn, direct		JC	LJMP
SUBB A, direct	MOV Rn, #data		JNC	SJMP
INC Rn	MOV direct, #data		JB	JMP @A+DPTR
DEC Rn	MOV DPTR, #d16		JNB	JZ
INC DPTR	MOVC (all)			JNZ
MUL AB	MOVX (all)			CJNE
	PUSH direct			DJNZ
	POP direct			NOP

7 Useability

Even though the remaining instruction set is somewhat rudimentary, it is still adequate for the Hitex In-Circuit-Emulators AX51, MX51, and DProbeHS to operate properly. So, the sample designs based on the Altera NIOS Hardware Design Kit and the Hitex In-Circuit-Emulators can be tried out with the evaluation version of QUIC_8051. However, it is not possible to execute the example programmes that come with the Hitex In-Circuit-Emulator. These example programmes are generated with a Keil C compiler and use library functions of it. These library function make excessive use of the whole instruction set and thus cannot be executed.

8 FPGA ressource usage

The FPGA resource usage of the evaluation version of the QUIC_8051 embedded processor core depends on the FPGA family used. A rough indication it can be derived from the fact that the evaluation version occupies approx. 2400 logic cells while the full version needs approx. 2700 logic cells in the example design described in application note Altera 001. Due to this reduced usage, the maximum frequency achievable with the evaluation version is approx. 10 % higher than with the full version.

9 ZIP content

For the different FPGA families different evaluation versions exist. The zip file usually contains:

- an EDIF net list
- (sometimes) a hex file as a part of the net list
- a 256 byte RAM module for the specific FPGA family.

For a quick evaluation, just copy the two or three files into the FPGA design directory.