QUIC_8051_OCD
Datasheet

Core release 1.0

Document release 0.3

Contents

1 Overview

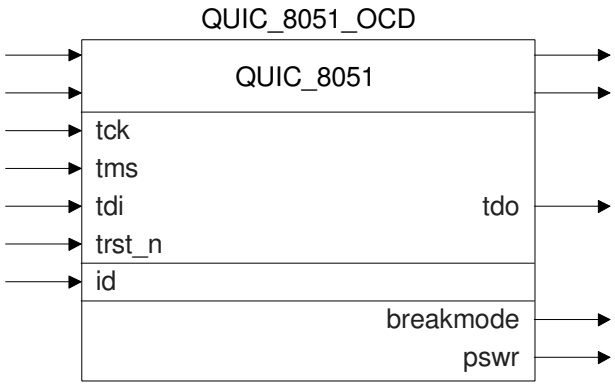
The QUIC_8051_OCD embedded controller core consist of a QUIC_8051 embedded controller core plus an extension for on-chip debugging that can be accesses though a standard JTAG interface. This document describes the debug extension only. Details about the controller core can be found in the associated documentation.

2 Top level view

This block diagram shows all additional input and output ports of the QUIC_8051_OCD module.

- JTAG signals
- identification
- additional control

Figure 1: Top level view



3 Interfaces

The tables below describe the additional input and output signals of the QUIC_8051_OCD. Low active signals are indicated with the suffix "_n".

3.1 JTAG port

Signal	Direction	Description
tck	in	These signals implement a standard JTAG port according to IEEE 1149.
tms	in	
tdi	in	
tdo	out	
trst_n	in	

Note that the trst_n signal is used as an enable signal for the on-chip debug module as well. Set trst_n to 1 in order to enable the debug module.

3.2 Identification

Signal	Direction	Description
id_version[3:0]	in	The IEEE 1149 standard requests an ID register for each TAP controller. QUIC_8051_OCD features separate port busses for each logic field of the ID register. These inputs must be hard wired to 0 or 1 in order to create the constant data for the ID register.
id_part[15:0]	in	
id_manufacturer[10:0]	in	

3.3 Control

Signal	Direction	Description
breakmode	out	This signal can be used to disable additional logic while the CPU is halted.
pswr	out	Program Store Write Enable

4 OCD (on-chip debug)

The on-chip debug module of the QUIC_8051 embedded processor core features all functionality needed for state-of-the-art debugging. This includes:

- start and stop of instruction execution
- read and write to processor register and memory
- breakpoint logic with comparators for code address

The on-chip debug module is accessed though a JTAG port according to IEE1149. In case of a breakpoint or a break request via JTAG the processor core is frozen. Read and write requests are processed by a dedicated spy module that does not alter the CPU status. Depending on the memory segment accesses are even possible in during program execution without real-time violation.

The breakpoint comparator register also are accessible via the JTAG port. So, these registers can also be programmed during program execution. A breakpoint only leads to a break if the address is read as a first instruction byte.

5 Communication

The on-chip debug module contains a TAP controller according to IEEE1149. There is an instruction register (IR) of 4 bit length and several data registers (DR) with different lengths. The instruction loaded into the IR determines which of the data registers is connected between TDI and TDO during a DR-scan.

6 Implementation hints

6.1 Write to program memory

Since a standard 8051 micro controller cannot write to C segment addresses a trick must help to load programs during debugging phase. For that, the 8051 embedded controller with on-chip debugging core features an additional signal named PSWR. This “program store write” signal is activated if a write to a C segment address takes place what can only be achieved through the JTAG interface. The timing of the signal is identical to that of the WR signal that denotes write to X segment addresses.

6.2 TRST_N

The input signal trst_n of the QUIC_8051_OCD should be routed directly to an input pin of the device. On the board there should be a weak pull down resistor of 10 kOhms or more. The signal must also be connected to the debug connector. This wiring scheme features two advantages.

If the SoC is used without a debugger device then the pull down applies a logic low level to the trst_n input. This disables the complete debug logic. So, it is assured that the logic does not influence the regulat behavior if the CPU.

If the SoC is used with an debugger device then this device ties the trst_n input to logic high level. This in turn enables the debug logic.