QUIC_8051
SFR table

Core release 1.0
Document release 0.9

1 List of all SFR

The table below shows all SFR implemented in the QUIC_8051 and their addresses in hexadecimal notation. It is not possible to add user SFR at addresses already occupied.

	x0	x1	x2	x3	x4	x5	x6	x7	0	
	x8	x9	xA	xB	xC	xD	xE	xF		8
8x		SP	DPL	DPH				PCON	0	
	TCON	TMOD	TL0	TL1	TH0	TH1				8
9x									0	
	SCON	SBUF								8
Ax	P2								0	
	IE									8
Bx									0	
	IP									8
Cx									0	
	T2CON		RCAP2L	RCAP2H	TL2	TH2				8
Dx	PSW								0	
										8
Ex	ACC								0	
										8
Fx	B								0	
										8

Shaded cells indicate bit-addressable SFR addresses. Seven of these addresses are available for user-added SFR.

2 List of all SFR bits

The tables below show the SFR bits implemented in SFR. Note that byte SFR like ACC, SBUF or the timer/counter registers are not listed here because their bits have no specific meaning.

TCON

SFR	7	6	5	4	3	2	1	0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TMOD

SFR	7	6	5	4	3	2	1	0
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
	Timer 1				Timer 0			

SCON

SFR	7	6	5	4	3	2	1	0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

IE

SFR	7	6	5	4	3	2	1	0
IE	EA	IE.6	ET2	ES	ET1	EX1	ET0	EX0

IP

SFR	7	6	5	4	3	2	1	0
IP	IP.7	IP.6	PT2	PS	PT1	PX1	PT0	PX0

T2CON

SFR	7	6	5	4	3	2	1	0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

PSW

SFR	7	6	5	4	3	2	1	0
PSW	CY	AC	F0	RS1	RS0	OV	PSW.1	P

Note that the SFR bits IE.6, IP.7, IP.6, and PSW.1 are implemented and can be written and read. However, there is no functionality assigned to these SFR bits.

For a detailed description of the SFR and SFR bits refer to the Intel Micro Controller Handbooks or to other literature about the 8051 family of micro controllers.